AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

1.- (Original) A two-dimensional matrix decoder for a digital-to-analog converter comprising an array of current cells, the cells having a current source means or a current divider means and a switching means, all cells being activatable in a pre-determined sequence,

the matrix decoder comprising:

a selection means outputting a first selection signal for selecting a cell,

a cell state signaling means outputting a cell state signal determining whether a cell comes before or after the selected cell in the pre-determined sequence,

matrix logic unit associated with each cell for generating a control signal suitable for controlling the switching means of that cell for switching current from the current source means or current divider means of that cell to at least one of a first node or a second node, the control signal being generated depending on the first selection signal and the cell state signal.

2.- (Original) A matrix decoder according to claim 1, wherein the selection means comprises a first decoder outputting a first selection signal for selecting a first set of cells, and a second decoder outputting a second selection signal for selecting a second set of cells, the first and second set of cells having the selected cell in common.

3.- (Original) A matrix decoder according to claim 2, wherein the first decoder is a row decoder and the first set of cells is a row of cells and the second decoder is a column decoder and the second set of cells is a column of cells.

4.- (Original) A matrix decoder according to claim 1, wherein the first node is an output node of the digital-to-analog converter and the second node is a ground node or dummy node of the digital-to-analog converter.

5.- (Original) A matrix decoder according to claim 2, wherein the first node is an output node of the digital-to-analog converter and the second node is a ground node or dummy node of the digital-to-analog converter.

6.- (Currently Amended) A matrix decoder according to claim 1, wherein the pre-determined sequence is such that a sequence of cells starts in the middle of the ~~matrix~~ array and expands from the middle to the sides of the ~~matrix~~ array.

7.- (Currently Amended) A matrix decoder according to claim 2, wherein the pre-determined sequence is such that a sequence of cells starts in the middle of the ~~matrix~~ array and expands from the middle to the sides of the ~~matrix~~ array.

8.- (Original) A matrix decoder according to claim 1, wherein the control signal generated by the matrix logic unit is suitable for controlling the switching means of that cell for switching current to either of a first, a second or a third node.

9.- (Original) A matrix decoder according to claim 2, wherein the control signal generated by the matrix logic unit is suitable for controlling the switching means of that cell for switching current to either of a first, a second or a third node.

10.- (Original) A digital-to-analog converter comprising:
an array of current cells, all cells being activatable in a pre-determined sequence,
a current source means or current divider means and a switching means, and
a matrix decoder in accordance with claim 1.

11.- (Original) A method for decoding a two-dimensional matrix for a digital-to-analog converter comprising an array of current cells, the cells having a current source means or current divider means and a switching means, all cells being activatable in a pre-determined sequence,

the method comprising:

selecting a cell,

determining whether a cell comes before or after the selected cell in the pre-determined sequence,

controlling the switching means of the cell for switching current from the current source means or current divider means of that cell to at least one of a first node or a second node, the controlling depending on whether the cell is selected or whether it comes before or after the selected cell in the pre-determined sequence.

12.- (Original) A method according to claim 11, wherein selecting a cell comprises selecting a first set of cells, and selecting a second set of cells, the first and second set of cells having the selected cell in common.

13.- (Original) A method according to claim 12, wherein selecting a first set of cells comprises selecting a row of cells and wherein selecting a second set of cells comprises selecting a column of cells.

14.- (Currently Amended) A method according to claim 11, wherein the pre-determined sequence is such that a chain of cells starts in the middle of the ~~matrix~~ array and expands from the middle to the sides of the ~~matrix~~ array.

15.- (Currently Amended) A method according to claim 12, wherein the pre-determined sequence is such that a chain of cells starts in the middle of the ~~matrix~~ array and expands from the middle to the sides of the ~~matrix~~ array.

16.- (Original) A method according to claim 11, wherein controlling the switching means comprises switching current to either of a first, a second or a third node.

17.- (Original) A method according to claim 12, wherein controlling the switching means comprises switching current to either of a first, a second or a third node.